

## DARPA-BAA-16-62

### Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)

#### Frequently Asked Questions

December 19, 2016

#### General Questions

Q: We requested a quote from an EDA vendor for a package to be offered to CHIPS performers, to include in our proposal. The vendor responded with a quote for each phase that were marked "Draft – For Budgetary Purpose Only" and said this was what they were providing to all the CHIPS proposers. The vendor claims this is acceptable to DARPA as a valid quote to use in the proposal. Please clarify whether this is indeed acceptable as a valid quote to use in the proposal submission.

A: This is acceptable as a vendor quote. Please include all technical and pricing assumptions that were used to generate the quote with the proposal, so that the Government can fully understand the pricing during source selection. Pricing marked this way would not be acceptable if the EDA supplier is a subcontractor on the proposal. In this case, the EDA supplier must provide a full quote like any other subcontractor.

Q: Are designs controlled by ITAR acceptable for CHIPS proposals?

A: Yes. It is the performers duty to comply with all ITAR requirements, but ITAR-restricted designs or technology may be included in CHIPS proposals. On a related note, CHIPS interface standards and public IP blocks are intended to be commercially available, and thus, cannot be ITAR-restricted.

Q: In looking at the BAA (amended version), the instructions for the Cost Proposal format on pages 26-30 do not include an explicit Section II. There is a Section I. Administrative and a Section III. Other Cost Information. Is Section II intended to be the editable Excel spreadsheet that we are to attach, with items A – J?

A: A header is missing from the BAA. The Section II header titled "Section II. Detailed Cost Information" should be at the top of page 27. This section encompasses the total program cost broken down by major cost items.

Q: Can you confirm that the final proposal deadline is now Jan 13, 2017?

A: Yes, the deadline per the BAA Amendment No. 01 is Jan 13, 2017.

Q: Are proposals targeted entirely to TA3 acceptable?

A: Yes, however TA3 work should be targeted to integrate with TA1 and/or TA2 developments on the program.

Q: The BAA does not provide a time frame for responses to the submitted abstracts. For our planning purposes, is there a window in which we should anticipate a response?

A: The abstract review process is still underway. Proposers will be notified as soon as reviews are complete.

Q: Given the timing for feedback on abstracts, will the due date for full proposals be changed?

A: Yes, we anticipate extending the proposal due date to January 13, 2017.

Q: We are in the process of writing a TA3 Abstract for the DARPA CHIPS BAA (DARPA-BAA-16-62). We have received some letters of support for our TA3. We were wondering if we could attach these letters to our abstract response. If so, would that count against our page total?

A: Yes, the letters of support may be included as attachments with both a proposal and an abstract. The letters will not count towards page limits.

Q: Is the 500 word Abstract "Submission Summary" publicly searchable?

A: No, proposal abstracts, full proposals, and related inputs are not publicly searchable.

Q: For the regular tech interchange meetings called out in the BAA, where should we assume they will be held?

A: This has not been determined yet, but plans for domestic travel should be included in cost proposals.

Q: Sec I.G GFP indicates that the gov't will provide access to wafer runs via the capabilities established in CRAFT, and that details and associated costs be included in CHIPS proposals. Are these costs to be simply referenced as associated gov't costs, or fully quoted and incorporated in cost and pricing data?

A: The proposal should document all costs associated with fabrication of chips. Pricing for access to the CRAFT run is available from MOSIS, as described in the separate CHIPS Update document.

Q: If a TAPO sponsorship is required for the CHIPS program, what is the procedure for obtaining the sponsorship?

A: TAPO sponsorship is not required for CHIPS. If a proposed process or application requires TAPO sponsorship, DARPA can support the request. Any such requests should be made directly to TAPO, and sponsorship will be provided by DARPA as needed.

## Interface Standards

Q: Do you intend to standardize the physical interface to chiplets – connection geometry, bump size, metallurgy, etc.?

A: The interface is expected to be standardized to the maximum extent possible in order to minimize the cost and time needed to incorporate additional or revised chiplets into an existing chiplet-based module. The exact content of this standard will be established in the program.

Q: In order to schedule our work, we need to know when the interface standard will be stable enough to incorporate into our design and fabrication for the 18-month demo. May we cost our proposal assuming that the interface specification(s) will be complete at 8 months and remain unchanged throughout the program?

A: The program schedule targets finalizing an interface standard by the CHIPS community at the 8-month milestone so that designs can be completed for the Phase 1 designs. Updates to this interface spec are possible based on initial results from Phase 1b that will then be held constant for both Phases 2 and 3.

## IP Block Considerations

Q: Would it be acceptable to deliver chiplets that use new or improved IP provided that the Government is not charged for the new IP development?

A: Yes, it is possible to propose new IP as part of a CHIPS solution. The government will assess the value of the IP inclusion against the increased risk of including unproven IP as part of an overall solution.

Q: In the event that a TA1 or TA2's proposed interposer technology is not considered to be compatible with the mutually agreed upon interface standard at the conclusion of Phase 1a, is that team necessarily downselected from the program? OR would that team proceed as a designer incorporating IP blocks onto a TA3 interposer (or potentially another TA1/TA2 interposer) that is compatible with the selected interface standard?

A: It is expected that proposed integration approaches will evolve on the program to enable convergence on a limited number of standard interfaces. Ideally, these CHIPS interface standards should be flexible enough to accommodate multiple substrate or interposer types. Finally, it is noted that there will not necessarily be just one interface standard.

Q: The metrics table that was discussed indicated that TA1 and TA2 teams must utilize >50% "public" IP blocks. Do these "public" blocks need to come from another CHIPS team (or a commercial entity), or can they come from one's own team as long as they are made "public" to other CHIPS performers? If they come from a sub to the prime of a team (and if they are made available to other CHIPS teams) are they considered "public"?

A: The blocks may come entirely from one's own team, but to be considered "Public IP", the blocks must also be made available to other performers and the proposal should document how that access is enabled.

Q: We have contacted Proposers B and C regarding potential availability of 'public IP' to accommodate the BAA requirement of 2-3 sources of IP from 'outside of the performer team'. In order to have a compliant cost proposal for TA1/TA2, must we:

a. Propose Proposers B and C as subcontractors with fully compliant subcontract bids incorporating all costing necessary to develop and fabricate that IP (even if Proposers B and C plan to propose identical development on their own TA1/TA2/TA3 prime proposals)?

b. Incorporate vendor quotes from Proposers B and C for purchasing or acquiring fabricated chiplets and leave the development cost to be bid separately in their prime bids?

If the answer is 'a', does that arrangement still meet the requirement of accommodating sources of IP from outside the performer team? If the answer is 'b', how should we accommodate the possibility that Proposer B or C are not selected in TA1/TA2/TA3?

A: Proposers should include all required costs in their cost proposal to ensure it fully complies with the BAA and, more importantly, from a cost and technical perspective, can stand on its own (i.e. proposals should not be contingent on the submission and/or selection of another proposal). If Performers B or C are also selected as independent prime performers, then DARPA will selectively fund proposal components to eliminate redundancy. It is noted, however, that "Public IP" should be available to CHIPS TA1 and TA2 performers, so the proposal should document how that access will be enabled.

## Modular Design and Integration

Q: We understand that in order to propose to TA1 or TA2, a team must bring to the table a "baseline" circuit which has already been designed, fabricated, and characterized, which is to be broken into blocks and reassembled through the course of the CHIPS program. It was clear from the proposer's day presentation that one option would be for this baseline circuit to be a monolithic "system on chip". However, many candidate circuits / subsystems, particularly for TA2 (e.g. T/R modules) employ some form of hybridization / heterogeneous integration (e.g. a "system in package"). Would such circuits be possible candidates for a TA1 or TA2 proposal as well, or must the "baseline" circuit be monolithic?

A: The baseline circuit does not have to be monolithic. CHIPS seeks to establish modular, reusable IP chipllets through interface standards. Existing non-monolithic circuits could be used as a starting point, and reconfigured into reusable blocks using the CHIPS interfaces selected during the program execution. However, the performance, cost and reusability benefits for a CHIPS instantiation beyond a conventional integration (e.g. multi-chip module or printed circuit board) should be made clear.

Q: Per the discussion in the Q&A session at the proposer's day, we understand that a TA1 or TA2 proposal should be self-contained in that all effort necessary to build, implement, and integrate all blocks necessary to meet the milestones should be included, but we understand that at the time of source selection, the government team may elect to fund development of only a subset of the blocks in such a proposal, specifying that other blocks will be produced by other teams and (presumably) provided as GFE (correct?). Is it possible that the government team may also elect not to fund the integration component of a TA1 or TA2 proposal, specifying that the block integration is also to be GFE, provided by another team?

A: It is correct that the government may elect to fund only select IP development costs. Regarding integration however, the Government does not intend to create a central foundry for integration or force performers to utilize integration by another team. However, proposers may find cost benefits to leveraging external resources (e.g., commercial integration foundries, or the DAHI foundry) that would increase the competitiveness of their proposal.

Q: For Phase III, >80% reuse is specified as a metric. Is this defined strictly in terms of block count (e.g. reuse of 4 out of 5 blocks would constitute 80% reuse), or defined in some more subtle way (e.g. in terms of total chip area)?

A: Performers should document how they expect to measure and achieve these reuse goals and the government will assess the value of the approach in light of the core program goals of speeding design time and lowering non-recurring engineering (NRE) costs.

Q: What is the expected maturity of the block integration method proposed to support a TA1 or TA2 (or even TA3) proposal (e.g. > TRL4)? Related to this, is some "hardening" of an integration method allowable within the scope of a TA1 or TA2 (or even TA3) proposal?

A: The program expects to leverage already demonstrated integration capabilities, so a higher TRL would be considered a strength. However, some interconnect development may be acceptable if it improves the performers' ability to meet program metrics.

## Eligibility and Teaming Questions

Q: A potential prime organization that is not equipped to handle ITAR is interested in teaming with an organization that has ITAR controlled demonstration capabilities that they believe DARPA would be interested in as part of later phases of the CHIPS program. What is the best avenue for the sub to share the ITAR controlled demonstration capabilities with DARPA that will not interfere with the prime's guardrail of not handling ITAR?

A: It is the performers duty to comply with all ITAR requirements, and the prime contractor is responsible for teaming on the proposal.

Q: Is it ok for a PI to be in multiple teams on different tasks (no overlap)?

A: The CHIPS BAA does not impose any particular restriction on teaming, and it is OK for an organization to submit multiple proposals.

Q: Can an academic institution take the lead to form a team? Or it is better for a university PI to be part of an industry team or defense contractor's team?

A: There is no requirement or preference on the type of affiliation of the PI for any technical area in the CHIPS BAA – the construct of the proposer's team will be assessed per the BAA (e.g., "Teaming and Management Plan").

Q: Do you recommend an EDA industry member in our team? How important is commercialization in CHIPS?

A: A portion of the performer responsibility in CHIPS is to establish a business model for a self-sustaining commercial effort post-CHIPS, so the potential for commercialization is considered an important part of the CHIPS program. See the evaluation criteria described in the BAA Part II Section V.A.e. A portion of this section reads, "A business model should be described for products and IP based on the BAA TAs, and the model will be evaluated for feasibility. Requirements for supporting interface standards should be outlined in the proposal, with the requirements described being evaluated for realism and sufficiency to support rapidly upgradeable IP." However, there is no requirement or preference on the affiliations of team members for proposals to any of the TAs.

Q: Would we be better off if we teamed with a larger company?

A: Although DARPA encourages teaming, company size and team size are not evaluation criteria. However, the performer's capability and related experience are included in the evaluation criteria - see the BAA Part II Section V.A for more details.

Q: In the eligibility section it states: "FFRDCs must clearly demonstrate that the proposed work is not otherwise available from the private sector; and (2) FFRDCs must provide a letter on official letterhead from their sponsoring organization citing the specific authority establishing their eligibility to propose to Government solicitations and compete with industry, and their compliance with the associated FFRDC sponsor agreement's terms and conditions. " Does it mean that the call is mainly targeted for the private sector?

A: No. As noted in the BAA, "all responsible sources capable of satisfying the Government's needs may submit a proposal that shall be considered by DARPA." However, FFRDC's, as well as Government entities, have certain statutory, regulatory and/or contractual conditions they must comply with in order to propose to a Government issued solicitation (in this case a BAA).

## Funding

Q: I could not find anywhere the approximate funding amount per project, also if the call is mainly targeted to individual or to larger teams.

A: The estimated total funding for the CHIPS program is included in the BAA Part I. The funding per project is dependent upon the scope, quality, and content of the proposals received and is expected to vary with project. Per the BAA Part II Section III.D.1, collaborative efforts and teaming for CHIPS proposals are encouraged. See also responses above regarding Eligibility and Teaming.